Calhoun
Institutional Archive of the Naval Postgraduate School

Calhoun: The NPS Institutional Archive

DSpace Repository

Theses and Dissertations 1. Thesis and Dissertation Collection, all items

1955

A study of factors limiting the utility of a digital memory system with nondestructive readout

Krohn, Stanley W.; Robinson, Thomas W.

Massachusetts Institute of Technology

http://hdl.handle.net/10945/14659

Downloaded from NPS Archive: Calhoun

DUDLEY KNOX LIBRARY

Calhoun is the Naval Postgraduate School's public access digital repository for research materials and institutional publications created by the NPS community. Calhoun is named for Professor of Mathematics Guy K. Calhoun, NPS's first appointed -- and published -- scholarly author.

Dudley Knox Library / Naval Postgraduate School
411 Dyer Road / 1 University Circle
Monterey, California USA 93943

http://www.nps.edu/library

A STUDY OF FACTORS LIMITING THE UTILITY OF A DIGITAL MEMORY SYSTEM WITH NONDESTRUCTIVE READOUT

Stanley W. Krohn

and

Thomas W. Robinson

Library
U. S. Naval Postgraduate School
Monterey, California

A STUDY OF FACTORS LIMITING THE UTILITY OF A DIGITAL MEMORY SYSTEM WITH NONDESTRUCTIVE READOUT

by

Stanley W. Krohn
U. S. Naval Academy (1950)

and

Thomas W. Robinson, III
U. S. Naval Academy (1950)

854
S

SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE
DEGREE OF NAVAL ENGINEER
at the
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
May 23, 1955

Signature of Authors. . . . .

. . . .
Department of Naval Architecture and Marine Engineering

Certified by. . . . .
Thesis Supervisor

Accepted by. . . . .
Chairman, Departmental Committee on Graduate Students

A STUDY OF FACTORS LIMITING THE UTILITY OF A DIGITAL MEMORY SYSTEM WITH NONDESTRUCTIVE READOUT

by

Stanley W. Krohn

Thomas W. Robinson III

(Submitted to the Department of Naval Architecture and Marine Engineering on 23 May 1955, in partial fulfillment of the requirements for the degree of Naval Engineer.)

ABSTRACT

The problem of determining the feasibility of expanding the system designed by General Electronics Laboratories, Inc., into a large practical array involves so many aspects that require concentrated study that this investigation was confined to a study and static analysis of the core and diode matrix scheme.

The immediately obvious problem was diode back leakage current. Whenever large numbers of crystal diodes are connected in parallel, the summation of individual back leakage currents at critical points may cause trouble by destroying stored information in a core, or by sufficiently reducing the net magnetizing force on the selected core so that proper readout is not insured. In addition, leakage currents generate directly on the output winding an unwanted voltage that may indicate wrong information when a core is read out.

To determine the size limitation imposed by the foregoing conditions, the diode matrix was analytically reduced, and the magnitude of total leakage current was calculated as a function of matrix size and read current. The pulse responses of the core used in the model in the "clear", "1", and "0" remanent states were then obtained for currents in the range of interest. The core response data was then correlated with the matrix analysis to find out which condition was the limiting one. Interpretation of the data was made under the assumption that the memory core and diode characteristics were identical.

The results included:

1) Leakage current output voltage is a function only of total leakage in a z - plane and is of the same sign as the readout voltage.
2) The use of silicon point - contact diodes allows a much greater matrix size.
3) For small disturbances, the magnitude of the output voltage of the core is independent of the state or the direction of the disturbance.

28791

The conclusions and recommendations included:

1) Leakage current output voltage is the factor that limits matrix size.
2) Good reliable operation may be obtained from a 32 x 32 size z - plane matrix.
3) The operation of a 64 x 64 size z - plane matrix would be marginal at best.
4) The existing device may not be operating under optimum conditions. At the read current value of 100 ma. used, the cores do not give the maximum difference between "1" and "0" readout voltages.
5) The use of clipping instead of reference core comparison technique, or the use of a reference core different from the memory core will greatly increase the limit to which the matrix may be extended.
6) A complete dynamic analysis should be made to determine if a limit is imposed by diode shunt capacitance and core inductance.

Thesis Supervisor: Thomas F. Jones, Jr.

Title: Associate Professor of Electrical Engineering

ACKNOWLEDGMENTS

In bringing this project to a close, it is with pleasure that we express our gratitude to those people who have contributed to the work involved. We are especially grateful to Professor Thomas F. Jones, Jr. for providing the stimulus which initiated this investigation. As thesis supervisor, he was helpful in more ways than can be told here.

We are also indebted to Mr. Bernard Widrow for his technical advice and assistance. His encouragement and foresight were instrumental in helping us to surmount many of the difficult, technical aspects which faced us.

Thanks are due Mr. William Hogan of Sylvania, Inc., Mr. Kenneth Perkins of General Electronics Laboratories, Inc., and to Miss Edith Repshis for her able secretarial assistance.

TABLE OF CONTENTS

Page

Title

Abstract

Acknowledgments

I Introduction. 1

II Procedure. 5

III Results. 6

IV Discussion of Results 7

V Conclusions. 15

VI Recommendations 16

VII Appendix. 17

- A. Details of Procedure 18
- B. Summary of Data and Calculations 24
- C. Sample Calculations 25
- D. Supplemental Discussion. 27
- E. Original Data. 29
- F. Bibliography 30

INTRODUCTION

The basis of the nondestructive readout method developed by General Electronics Labs. Inc., and tested in a sixteen word breadboard model is minor loop permeability. Bozorth (1) shows how minor loop permeability varies for different remanent states. For a stable remanent state near the maximum negative remanent state, the ratio of minor loop permeability to the permeability at the undisturbed zero (maximum positive remanent) state is approximately 2 to 1.

In Fig. I, stable remanent state "A" is defined as a "1". Normally, maximum negative remanence is given this designation, but in order to proceed logically from the work already done on this method, the notations previously established will be continued. If a core in state "1" is pulsed positively to H', the magnitude of the output doublet voltage which appears across secondary windings will be approximately twice the voltage that would appear if the core were in the "0" state. Since state "1" is stable, a readout pulse of magnitude H' may be applied an infinite number of times without destroying the state, and the intelligence stored by the core may be determined by the secondary voltage magnitude. The advantages of this nondestructive readout system over the presently used read - rewrite system of coincident currents is felt not to be a part of the objectives of this investigation.

Two practical ways of differentiating between the "1" and "0" read voltages are clipping and reference core comparison. In the first,

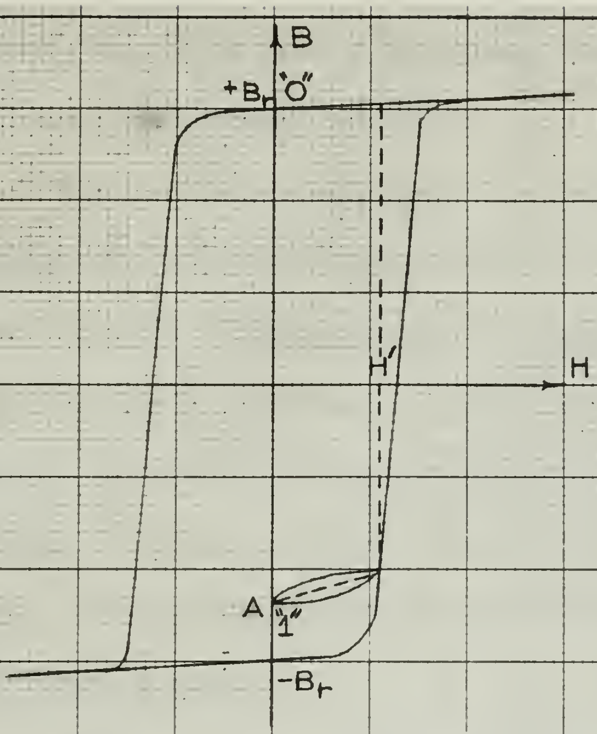


FIGURE I
D.C.
HYSTERESIS LOOP

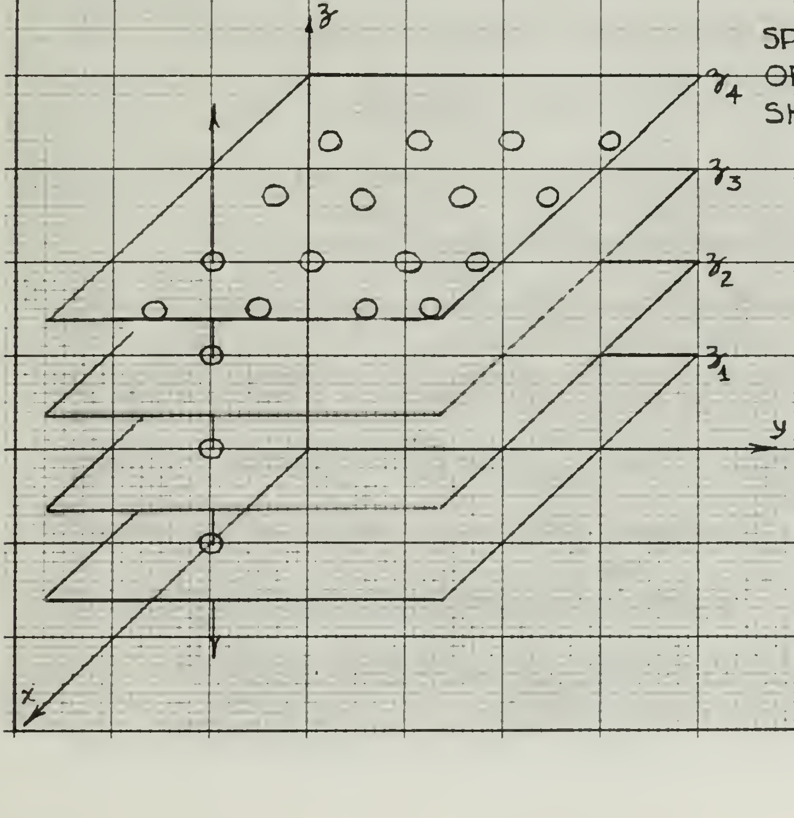


FIGURE II
SPACIAL CONFIGURATION
OF THE CORE MATRIX
SHOWING WORD (x_3, y_1)

the maximum "0" output voltage would be determined, and circuits would be designed to exclude all signals below that level. In this manner, the output from a stored one would yield a signal but the output from a stored zero would not.

The second method compares the output of the memory core with that of a reference core which is always in the zero state. The cores are pulsed identically and simultaneously, and the outputs are fed to a difference amplifier. If the memory core holds a zero, the comparison with the reference core in the difference amplifier will theoretically yield no output, whereas if it holds a one, there will be an output. General Electronics Labs. chose this method in constructing their working model.

To show how a memory matrix may operate on this principle of nondestructive readout, a 4 by 4 by 4 matrix will be used as an illustration. Fig. III is the circuit diagram of the memory. Included on this figure are wiring diagrams for both the reference and memory elements. Fig. II shows the spatial configuration of the matrix.

The matrix capacity is sixteen words of four binary digits per word. The four cores with the same (x, y) coordinates in all four z - planes make up one word. The X and Y drivers work in pairs, so that the selection of drivers X_n and Y_m pulses the word (x_n, y_m). Each word has a reference core associated with it, and each core has a forward and back diode associated with it.

Pulsing a word through the "clear" circuit sends a 100 ma. pulse through twenty turns on each core in the word, and drives them all into

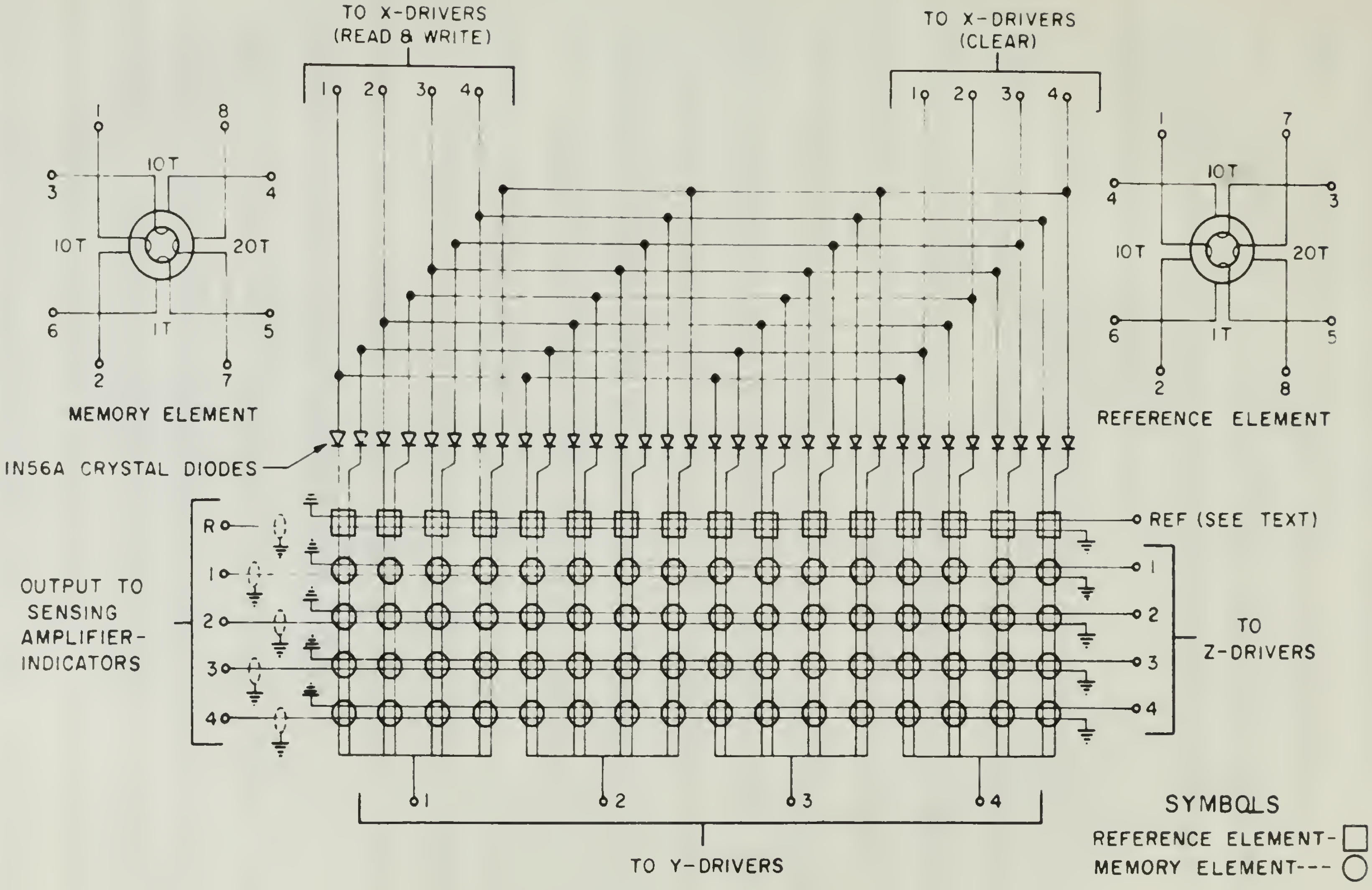


FIGURE III - CIRCUIT DIAGRAM OF REGISTER FOR STORAGE OF 16 4-BIT WORDS

the maximum negative remanent state. At the same time, reversed current connections on the reference core associated with the word drives it into the "0" or positive remanent state. The clear condition, then, is all memory cores in the maximum negative remanent state and the reference core in the "0" state.

To write a "0" into a memory core, the appropriate X, Y, and Z drivers are energized. The X and Y drivers in combination, and the Z driver, each supply 100 ma. through ten turns and switch the designated core into the "0" state. All other cores in the z - plane and all other cores in the word are disturbed from the clear state into the stable "1" state by a magnetizing force of one ampere - turn, since the Z driver selects an entire plane and the X and Y drivers select a whole word. The reference core state is not disturbed because the write - zero pulse is in the positive direction, i.e., in such a direction as to drive it further into the "0" state.

Writing a "1" into a core merely requires that the core be disturbed by 100 ma. through ten turns. Ones are written into whole words at once by selection of appropriate X and Y drivers.

Similarly, in reading out, an entire word is read out at once. Each z - plane has its own output winding which threads all cores in that plane. A selected combination of X and Y drivers pulses a word and its reference core with one ampere - turn. This amplitude read pulse will not disturb cores from their stable states. One core in each z - plane is therefore energized, and the output of each z - plane is

compared, in a difference amplifier, with the voltage output of the "0" state reference core of the selected word. This readout process may be repeated an infinite number of times without destroying the intelligence on the cores. Reading out and writing ones are identical operations insofar as the drivers are concerned.

For further information concerning the actual circuits and operation of the breadboard model constructed by General Electronics Labs. Inc., see (2).

The Diode Matrix

Fig. III shows that paralleling the core matrix is a diode matrix, the purpose of which is disassociation of the "clear" and "read - write" circuits. Since the diodes are not perfect, some leakage occurs. As the matrix is expanded in size, more back paths through the diodes are put in parallel, increasing the total leakage current. These individual back leakage currents may combine at points in the matrix. If the combined leakage current is sufficiently large, it may cause trouble in three ways. It may disturb the remanent state of a core. It may generate an unwanted voltage directly on the output winding that causes the indication of wrong information. Finally, it may reduce the net magnetizing force on the selected core sufficiently so that its "1" voltage output when readout cannot be differentiated from the "0" output of the reference core.

PROCEDURE

The diode matrix in Fig. III was redrawn in three dimensions without the cores as shown in Fig. IV-A. When the assumption is made that all diodes are identical, it is possible to reduce the three dimensional matrix of Fig. IV-A to the simple parallel circuit of Fig. V-A. Use of this circuit in conjunction with forward and reverse low voltage characteristic curves for the 1N56A (the diode employed by the system under consideration) permitted the calculation of leakage current versus read current for various values of matrix size.

The voltages on core output windings for low ampere - turn inputs were obtained in the laboratory. A continuous spectrum of this leakage voltage was obtained for the three different states in which the core could be, the clear state, the "1" state, and the "0" state.

The matrix leakage paths were analyzed to determine the locations of the "critical" points where all or many of the individual leakage currents combined.

The laboratory data was correlated with the diode matrix analysis and the leakage path analysis to estimate to what approximate size the matrix could be extended before one of the three troubles previously mentioned blocked a further increase in size.

FIGURE IV A
THREE DIMENSIONAL
VIEW OF DIODE MATRIX

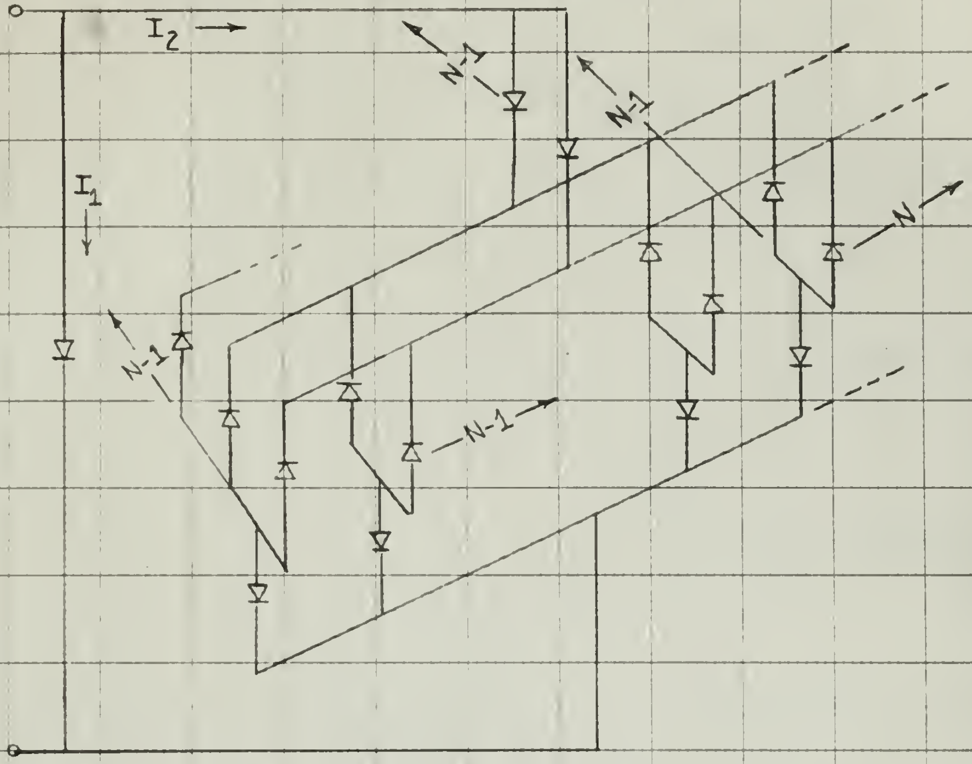


FIGURE IV B
LEAKAGE CURRENTS
SELECTED WORD X$_1$Y$_1$

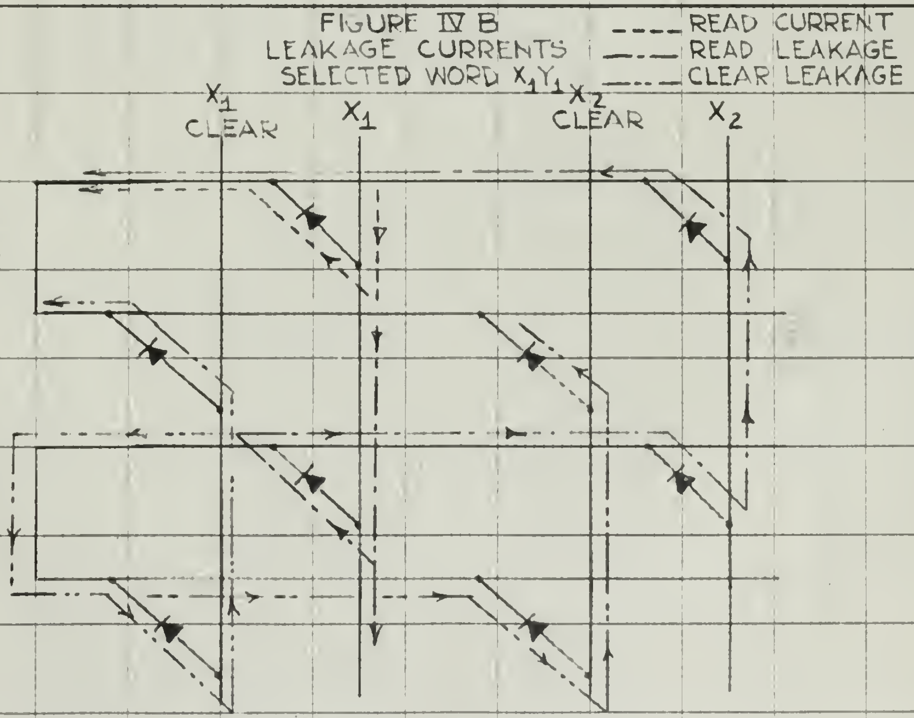


FIGURE V A
REDUCED DIODE MATRIX

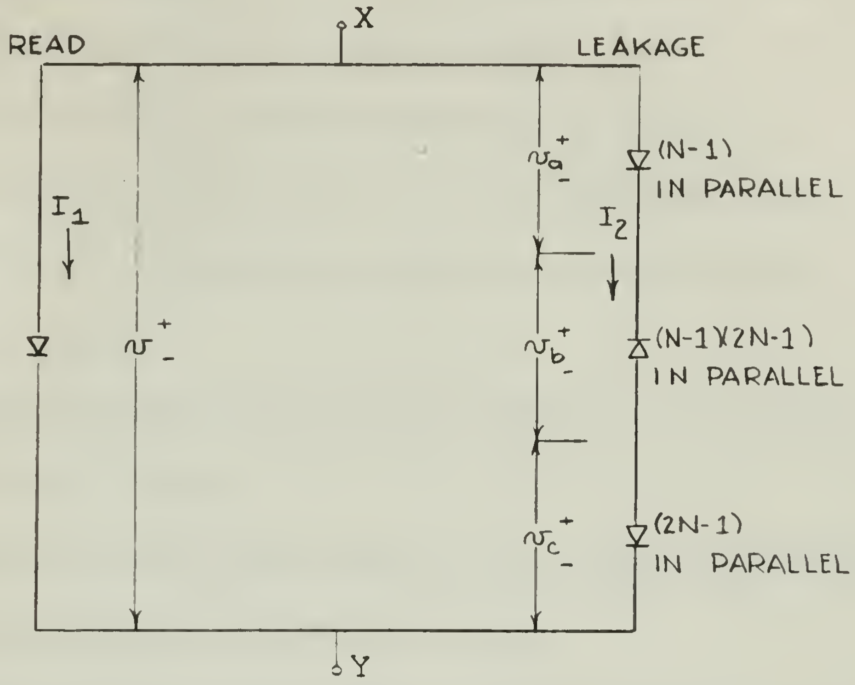
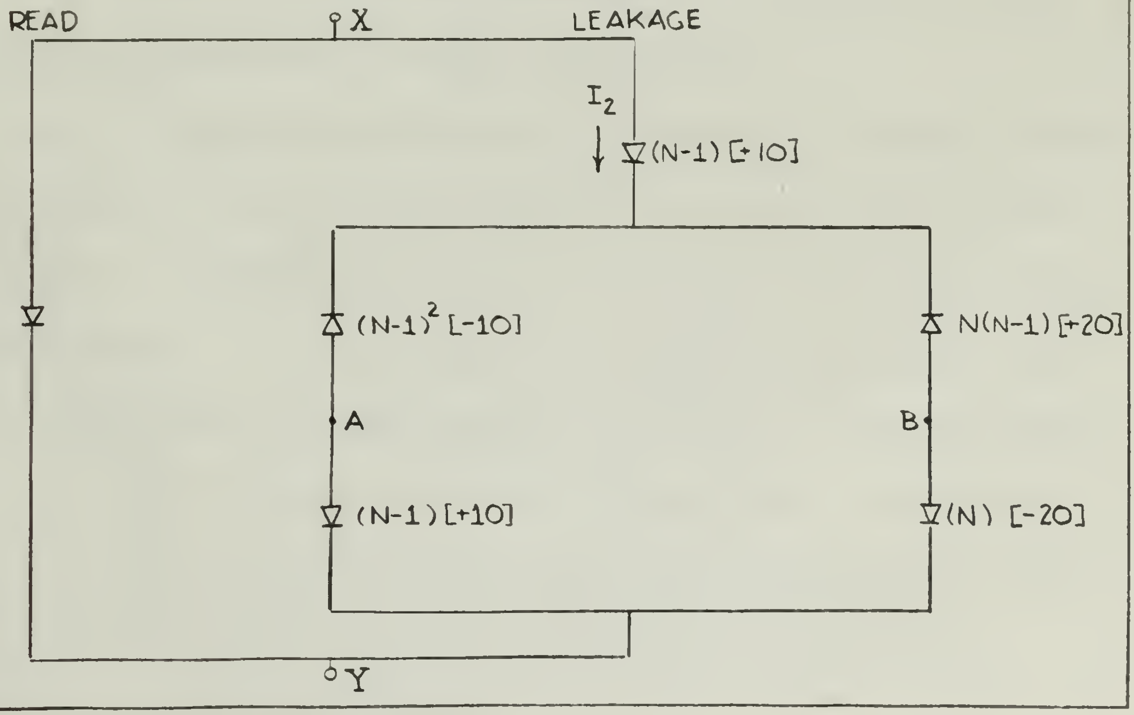


FIGURE V B
REDUCED DIODE MATRIX
WITH CORE WINDINGS
AND DIRECTION



RESULTS

1) For small ampere - turn magnetizing forces, the magnitude of the voltage output of the core is independent of the state of the core or the direction of the magnetizing force. Fig. VI shows the voltage output curves for a core in the "1", "0", and "clear" states when pulsed positively. The curves are identical up to a value of about .2 ampere - turns.

2) Leakage current output voltage is a function only of total leakage current in a z - plane.

3) Leakage current output voltage is of the sense to add to the "1" and "0" output in the z - plane output winding.

4) Leakage current output voltage is independent of the "z" direction of expansion.

5) Total leakage current increases with an increase in read current or matrix sizes. See Figs. VII and VIII-A.

6) A selection magnetizing-force current of 1.1 ampere - turns yields a higher "1" to "0" output ratio than 1.0 ampere - turns used in the system. The plot of the output curves for these two remanent states is shown on Fig. VI. Increasing the read current to some higher value will ease the problem of differentiating between the 1" and "0" outputs.

7) Fig. VII shows one curve for silicon diode, Transitron type S-5. The leakage currents computed for a 256 x 256 size matrix using these diodes are less than those in a 50 x 50 size using the 1N56A.

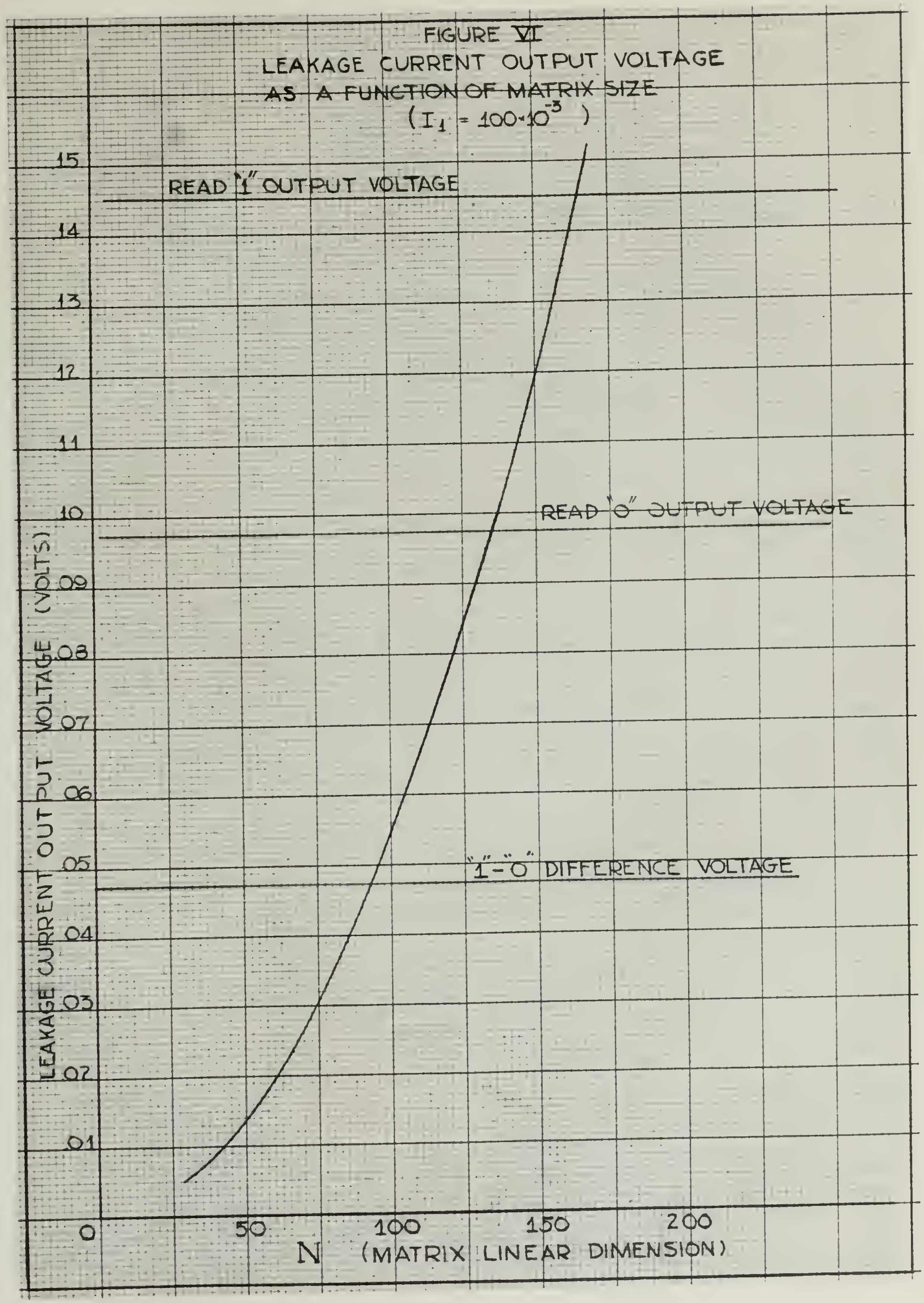


FIGURE VI
LEAKAGE CURRENT OUTPUT VOLTAGE
AS A FUNCTION OF MATRIX SIZE
$(I_1 = 100 \cdot 10^{-3})$

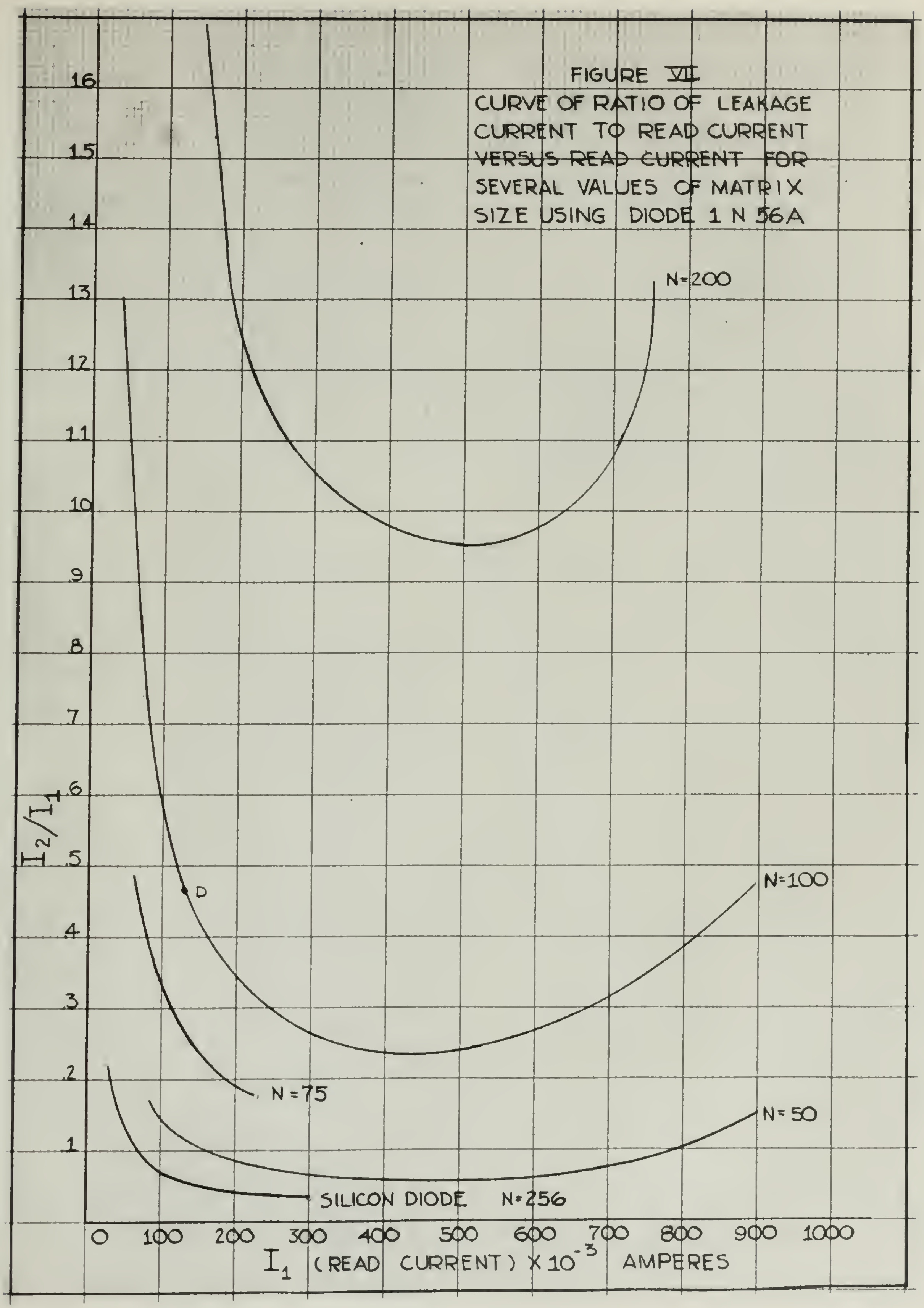


FIGURE VII
CURVE OF RATIO OF LEAKAGE CURRENT TO READ CURRENT VERSUS READ CURRENT FOR SEVERAL VALUES OF MATRIX SIZE USING DIODE 1 N 56A

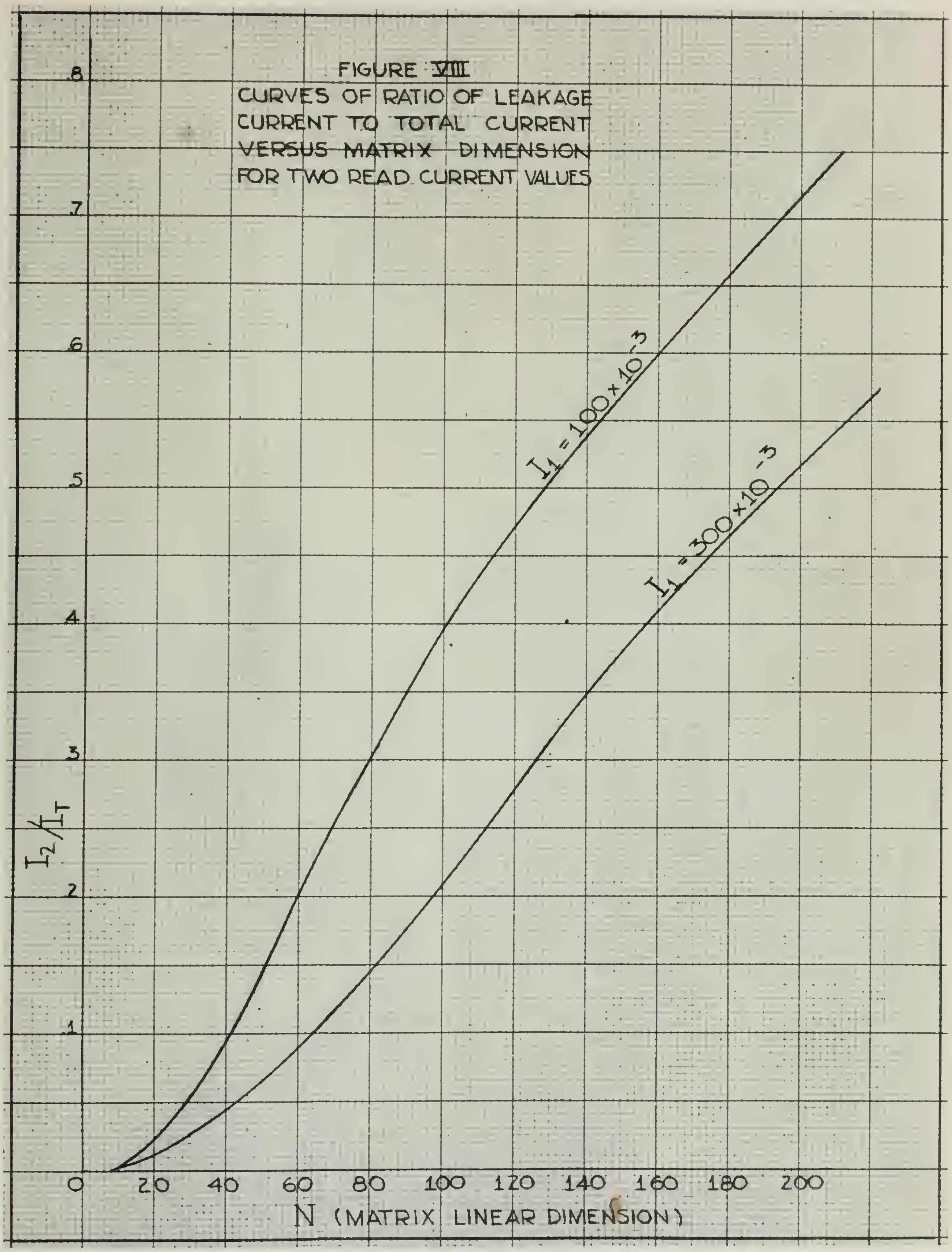


FIGURE VIII
CURVES OF RATIO OF LEAKAGE CURRENT TO TOTAL CURRENT VERSUS MATRIX DIMENSION FOR TWO READ CURRENT VALUES

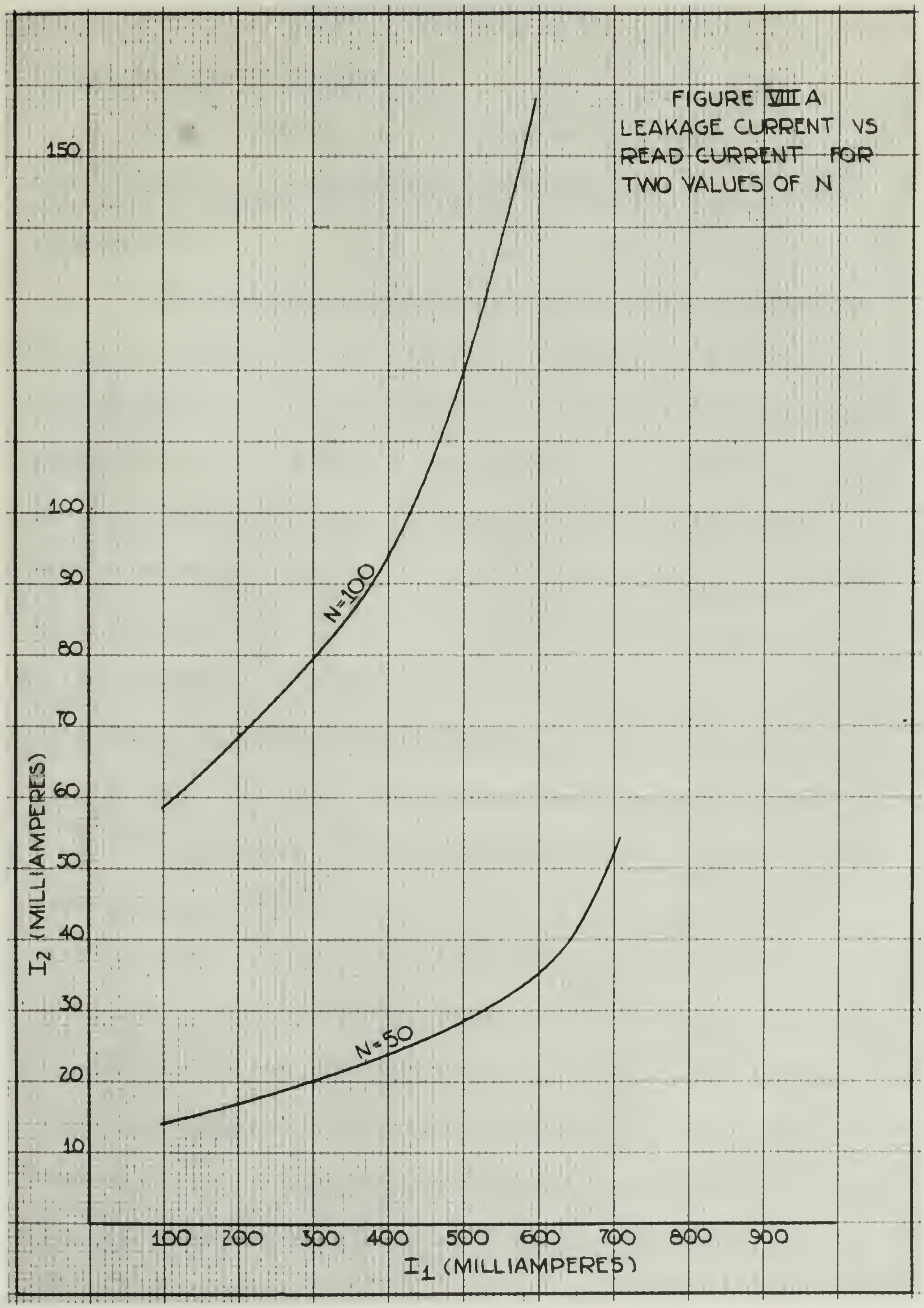


FIGURE VIII A
LEAKAGE CURRENT VS
READ CURRENT FOR
TWO VALUES OF N

DISCUSSION OF RESULTS

Matrix Analysis of Leakage Paths

The exact locations of anticipated trouble conditions were established in general terms by analysis of the leakage paths shown in Fig. IV-B.

If the word at (x_1, y_1) was selected to be read, all cores in every x - position on the y_1 line, except the selected core, could have its remanent state sufficiently disturbed so that the output voltage would indicate a "1" when a "0" was actually stored. This is seen by observing that the magnitudes of the leakage currents through the "clear" and "read" windings of cores in positions ($x_{2, 3 \ldots n}$, y_1) are approximately equal. The "clear" winding has twice as many turns as the read winding. Therefore, the net effective magnetizing force on the core is from the leakage current in the "clear" winding which tends to disturb the cores toward the negative remanent or "clear" state. If the core is disturbed sufficiently (not necessarily all or even most of the way to the "1" state) its output voltage when read at a later date could be large enough to indicate a "1".

It is also seen that the same magnitude of leakage current in the above "clear" windings also flows in the "clear" winding of the selected core. If this leakage current is sufficiently large, it may reduce the net read magnetizing force to such a value that a "1" output voltage is reduced so that it may not be differentiated from the "0" voltage of the reference core.

However, if these leakage currents are traced back through their paths, it is established that the sum of both the "clear" and "read" leakage currents at $(x_{2,3\ldots n}, y_1)$ flows through read windings at core positions $(x_1, y_{2,3\ldots n})$. The effect of these currents is to generate an unwanted positive voltage on the output winding. If the selected core stores a "0", this leakage current voltage adds to the "0" output voltage from the z - plane and the sum may be sufficiently larger than the reference core "0" voltage to indicate a "1". It is very important to note that this leakage current voltage also adds to a "1" output voltage of the z - plane.

Let I_1 equal the read current, I_2 equal total leakage current, I_c equal leakage current in "clear" winding of the selected core, and n equal linear dimension of matrix size.

Then for $n = 75$ (75 x 75 matrix), at $I_1 = 100$ ma., $I_2 = 33$ ma. The maximum leakage current in the "clear" winding of the selected core is $\frac{I_2}{2n-1} = \frac{33}{149} = .2215$ ma. The ratio of $\frac{I_1}{I_c} = \frac{100}{.2215} = 452$.

For $\frac{I_1}{I_c} = 100$, the ratio of; $\frac{\text{net magnetizing force on the core}}{\text{magnetizing force from } I_1 \text{ alone}}$ is .98 (I_c flows through twice as many turns). Since the read $H = 1$ amp.-turn, the net H on the selected core equals .98 amp.-turns. This reduces the magnitude of the "1" output voltage by only $\frac{1}{200}$ of a volt or 5 mv. (from Fig. IX-B). Since the ratio, $\frac{I_1}{I_c}$ for $n = 75$ is more than four times 100, the ratio of magnetizing forces is even closer to

FIGURE IX A
BLOCK DIAGRAM OF TEST EQUIPMENT FOR DETERMINING SMALL ~~NOISE~~ CORE VOLTAGES

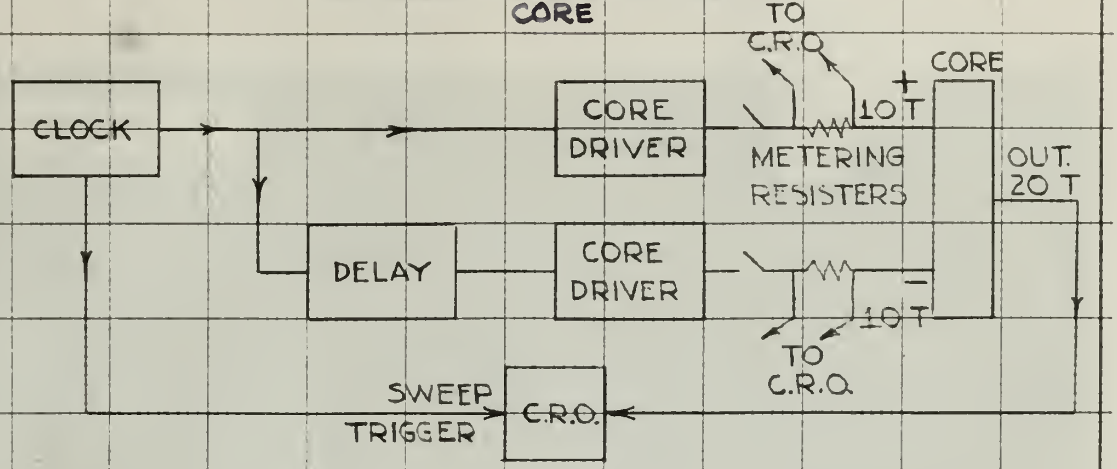
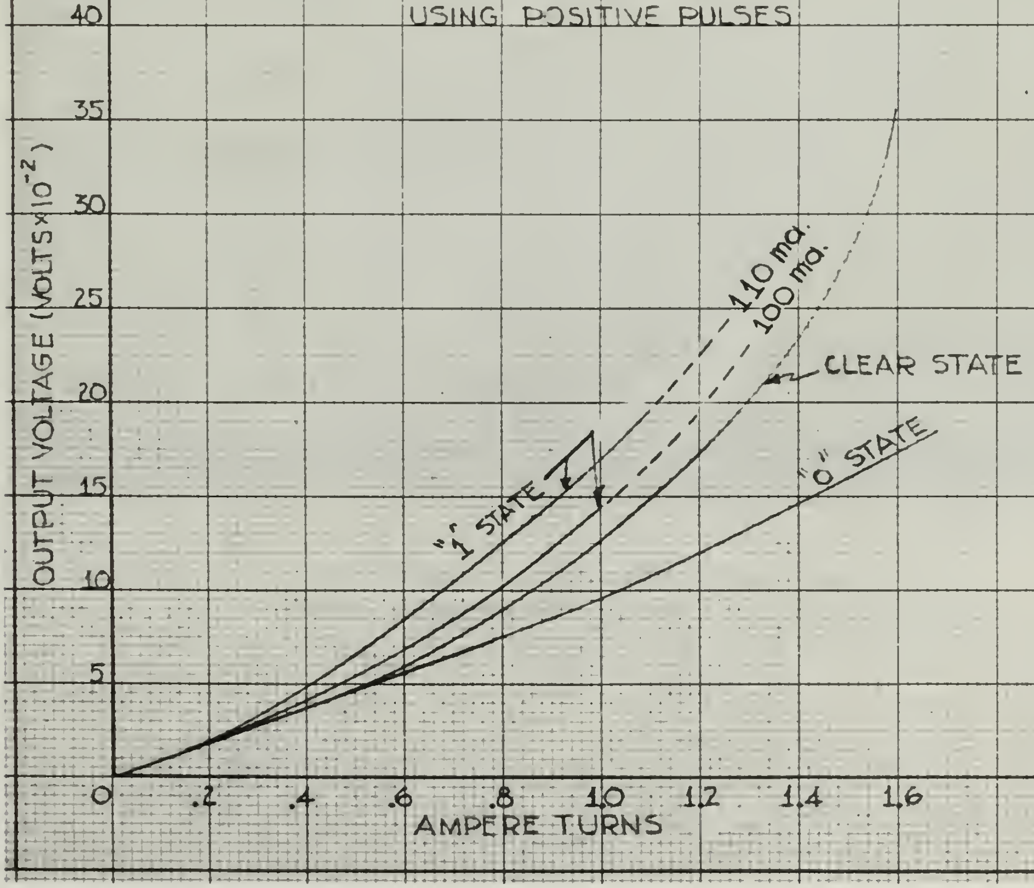
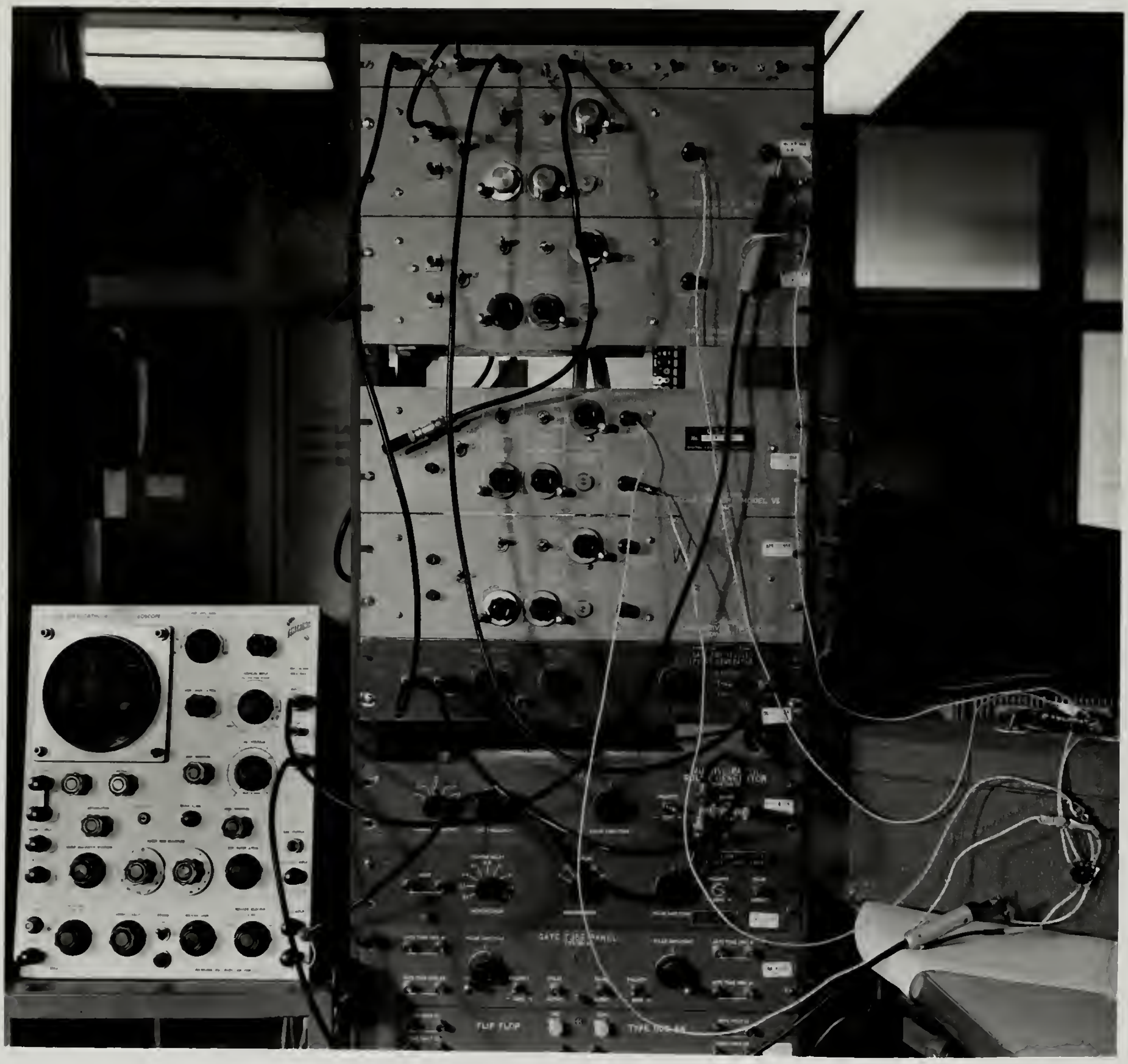


FIGURE IX B
SINGLE TURN OUTPUT OF MEMORY CORE FOR DIFFERENT CORE STATES USING POSITIVE PULSES





Test Equipment Set-Up for determining small [redacted] voltages from memory cores.

1.0. A matrix of $n = 75$ is already past what is considered marginal operation by reason of leakage output voltage. (See Correlation of Core Data with Matrix Analysis). Therefore, it is determined that this situation need not be a consideration in expanding the presently existing system, since its size is already limited by another effect of leakage current.

The leakage current through "clear" windings may destroy information if large enough. Let $I_2 = 33$ ma. ($n = 75$, $I_1 = 100$ ma.). The H applied to the cores at $(x_{2,3\ldots n}, y_1)$ from the leakage current in the read winding is: $\frac{I_2}{2n-1}$ (10 turns). From the clear winding: $\frac{I_2}{2n-1}$ (-20 turns).

The net H is the sum of the above:

$$\text{Net } H = \frac{I_2}{2n-1}(10 - 20) = -2.215 \text{ ma. turns.}$$

This is much too small to disturb the remanent state sufficiently to increase the output voltage of a core when read out at a later date. Again matrix size is already limited by another effect of leakage current.

Matrix Analysis of Diodes

Total leakage current was found to be a function of I_1 the selection current, n the linear dimension of matrix size, and the characteristics of the particular diodes used. Forward and reverse low voltage characteristics of the Sylvania 1N56A, the diode used in the system under consideration, obtained from the manufacturer

(Figs. X and XI) permitted the calculation of the magnitude of total leakage current for any matrix size and given value of I_1. These results are plotted in several different forms in Figs. VII, VIII, and VIII-A. The curves show both the manner in which total leakage current increases with matrix size and magnitude of read current, as well as the relative & absolute magnitudes of total leakage current. A significant system improvement was noted over the germanium diodes with the use of a silicon diode, Transitron type S-5. It was necessary to increase the matrix size to 256 x 256 in order to obtain leakage current magnitudes to permit plotting on the same scale of Fig. VII.

Memory Core Characteristics

Theoretically, core output voltages should depend on the remanent position of the core on its hysterisis loop, being proportional to the incremental permeability at each remanent position. When output data was taken for the three possible remanent states of the cores as used in this system, it was found that the curves of output voltage versus magnetizing force were coincident up to a magnetizing force of about .2 amp.-turns. It is felt that the reason for this lay in the accuracy limitations of the test equipment rather than the actual core characteristics being identical for all three remanent states. In the measurement of the extremely small output voltages from the small magnetizing forces which would result from the magnitudes of leakage currents found in the diode analysis, differences in

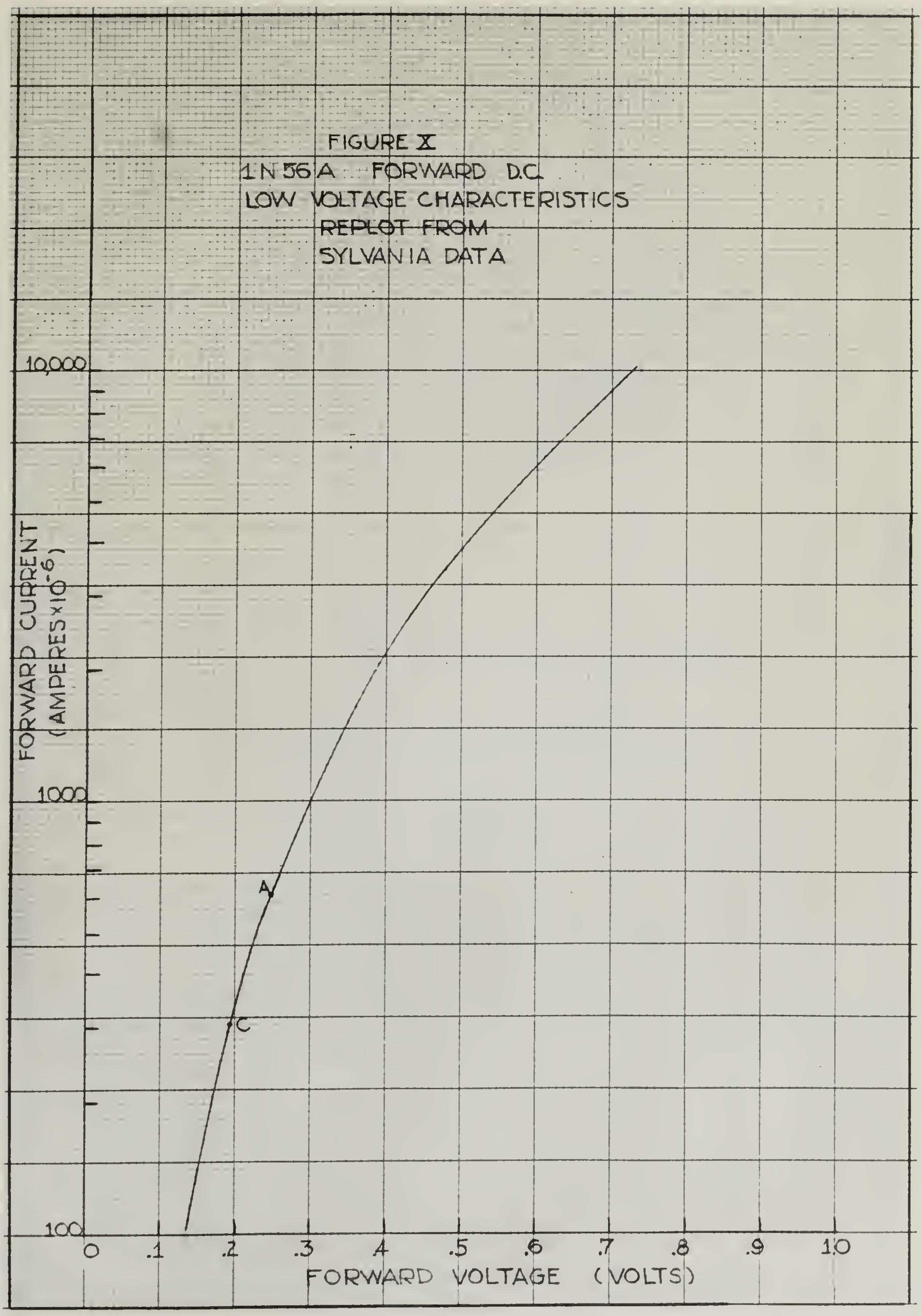


FIGURE X
1N56A FORWARD D.C.
LOW VOLTAGE CHARACTERISTICS
REPLOT FROM
SYLVANIA DATA

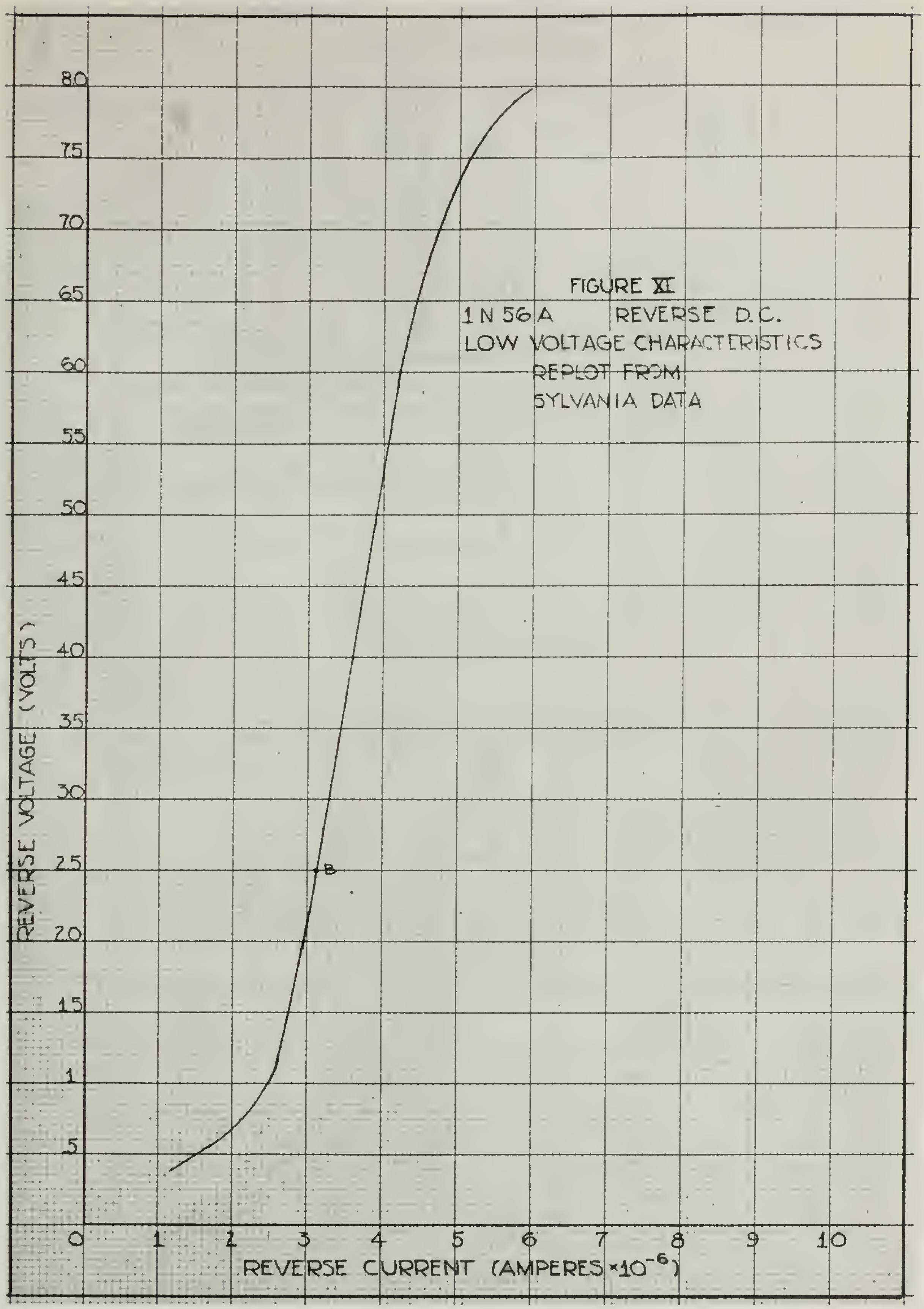
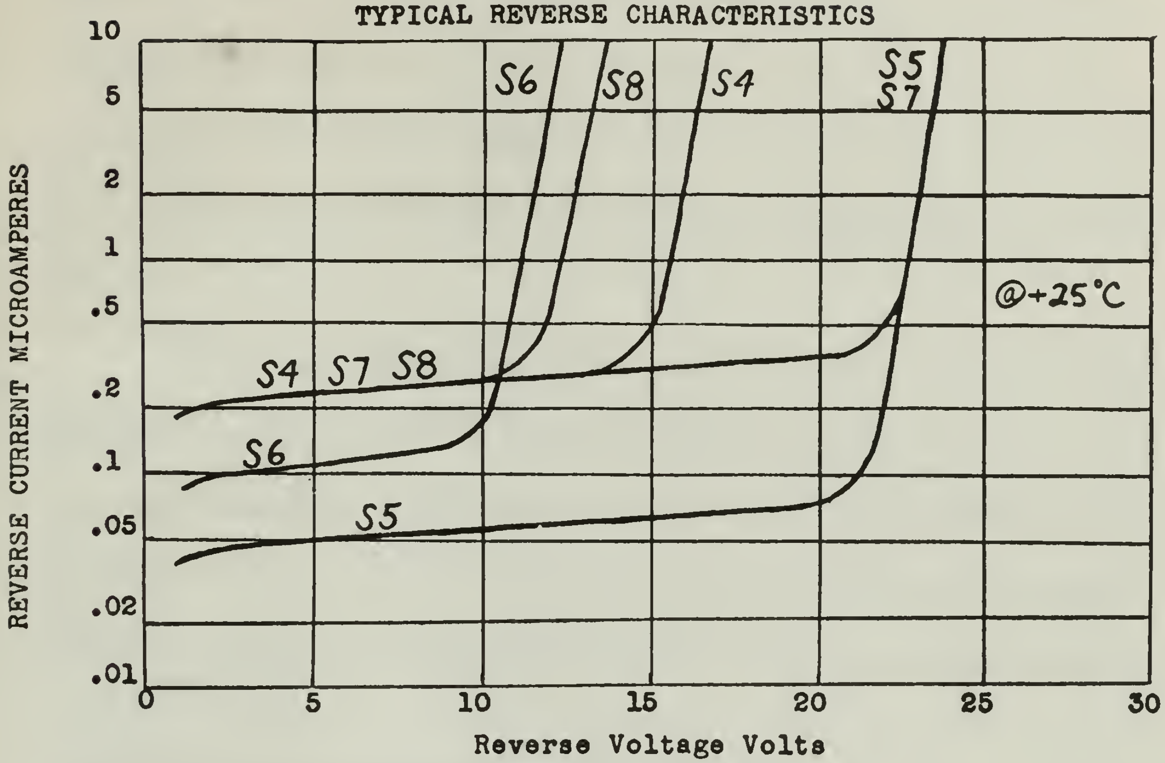


FIGURE XI
1 N 56 A REVERSE D.C.
LOW VOLTAGE CHARACTERISTICS
~~REPLOT FROM~~
SYLVANIA DATA

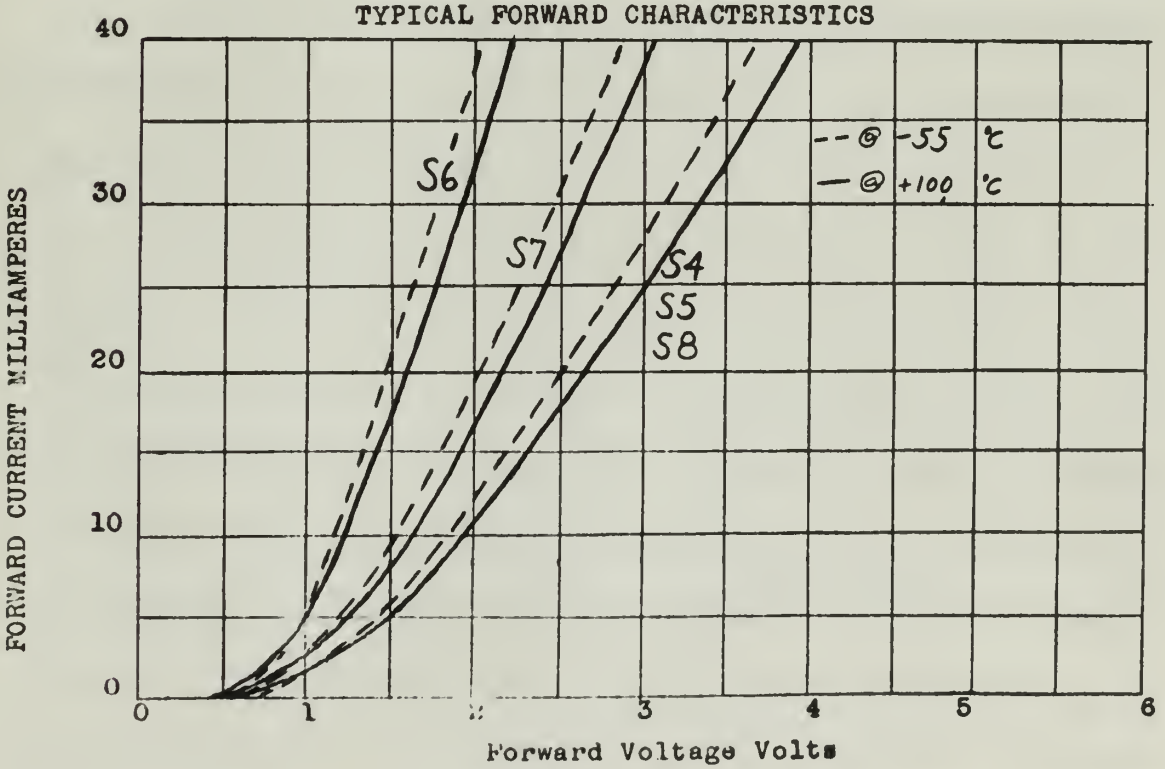
FIGURE XII COURTESY OF TRANSITRON ELECTRONIC CORPORATION

BONDED SILICON DIODE

TYPICAL REVERSE CHARACTERISTICS



TYPICAL FORWARD CHARACTERISTICS



output voltages between the core states were not measurable. Because of this, and since the output voltage curves appeared to be coincident near the origin, with a constant slope, the assumption was made that any actual differences of output voltage for the remanent states would be negligible up to a magnetizing force of .2 amp.-turns.

When the magnetizing force was increased to values near the region of operation, it was found that an appreciably higher "1" output was obtainable. The response of a "1" for a read current of 110 ma. was plotted on Fig. IX-B to illustrate this. Bozorth (1) shows how incremental permeability varies for different remanent states.

Correlation of Core Data with Matrix Analysis

Every core with leakage current in it will generate a voltage on an output winding. A general analysis of the matrix using established magnitudes of leakage current, core voltage output data, the equivalent circuit of Fig. V-B, and the number and direction of core windings, was made to determine a final magnitude of output voltage from leakage current. It was found that all the leakage voltages from cores associated with the two parallel branches cancelled, leaving as the only leakage output voltage that generated by the cores associated with the set of forward diodes in series with the parallel branches of Fig. V-B. These cores, in the case of a selected position of (x_1, y_1), are at the $(x_1, y_{2,3...n})$ positions previously mentioned. In general

terms, for a selected position of (x_n, y_m) all cores on the x_n line, less the selected core, will generate output voltages from leakage currents.

The magnitudes of leakage output voltages for a series of leakage currents, which were identified with matrix sizes by holding I_1 constant at 100 ma., were calculated and plotted against matrix size in Fig. VI. In addition "1", "0", and "1" - "0" voltage magnitude levels were drawn on the same figure.

As previously noted, the leakage current output voltage is added to both the "1" and "0" output voltage from the memory cores. However, the magnitude of the reference core "0" response is fixed. This means that if a 0" is to be read out of a memory core, leakage current output voltage may add a sufficient amount to the total output voltage to have the sensing amplifier indicate a "1" response. The matrix size 64 x 64 was determined to be marginal by the following somewhat arbitrary reasoning.

This is the size where the "1" - "0" difference voltage is reduced by approximately one half, and it will be reduced even more by statistical variations in core and diode characteristics. Consistent detection of ones and zeros with very small difference voltages requires extremely careful engineering of sensing amplifiers with precision components. This is the major limitation when it is kept in mind that consistent, reliable detection is of paramount importance.

Noise Voltage Considerations

It should be noted that these leakage output voltages are predictable to the extent that the diode and core characteristics are identical. Random, unpredictable voltages, commonly known as "noise" voltages, will exist in this system and may ultimately limit the matrix size.

Several possible sources of noise voltage exist. A diode may change its characteristics after a period of operation and permit more leakage current in a leakage path. This means that there may be incomplete cancellation of the leakage voltages generated in the matrix positions other than cores on the selected x - line, y - positions. These are random because the effect could be any of the ones discussed previously, depending on the particular diode that is bad.

Cores will undoubtedly be individually tested (automatic or otherwise) to obtain as nearly uniform responses as possible. Nevertheless, small differences will exist simply because obtaining exactly identical cores in large numbers is a tremendously difficult problem. The differences in core responses will again result in incomplete leakage current output voltage cancellation, even if all diodes are exactly identical. As before, these uncancelled leakage output voltages are random and unpredictable.

There is always the possibility of spurious voltages being

generated from air leakage flux, and other energy fields from external sources.

It is obvious that as matrix size increases,the opportunities for generation of noise voltages will increase. No quantitative estimates or predictions can be made except by measurements as larger and larger matrices are operated.

CONCLUSIONS

1) In the range of matrix sizes investigated, magnitudes of leakage current are too small to be the limiting effect by preventing proper readout of the selected core or destroying stored information. The present system, then, is limited in size by the leakage current output voltage which adds to the "0" readout to indicate a "1".

2) Expansion of the present system to a 32 by 32 matrix is feasible since at this matrix size, the leakage current output voltage is only 15 percent of the "1" - "0" output voltage difference. At 64 by 64, however, the percentage is more than 50 percent, and operation is marginal at best.

3) The system may not be operating at its optimum point, since 100 ma. read current does not yield the maximum "1" to "0" output ratio. For each value of matrix size, the read current value must be optimized to give the maximum "1" - "0" output voltage difference with minimum leakage current.

RECOMMENDATIONS

1) In the existing system, there always will be a difference between the "0" readout voltage and the reference core output voltage. This difference is the leakage voltage. If a core larger than the memory core is used as reference, the voltage output of the reference will be larger and may be used to compensate for the leakage voltage. Overcompensation, or designing the reference output to lie between the "1" and "0" readout voltages, will ease the problem of subsequent amplification of the output difference.

2) The use of clipping to differentiate between the "1" and "0" output should also be thoroughly investigated.

3) The system should be operated at a point of maximum "1" to "0" output voltage difference, and input turns (read current magnitude) should be adjusted within practical limits for minimum leakage current.

4) The use of smaller memory cores may greatly reduce the problem of winding the cores by reducing the number of windings. This, however, may reduce the "1" to "0" output difference, thereby making differentiation between the two signals more difficult.

5) It is of the utmost importance that a dynamic analysis of the system be made. The further limitations imposed by stray capacitance, diode shunt capacitance, and other dynamic factors may be extreme.

6) The use of silicon point-contact diodes is highly recommended.

APPENDIX

APPENDIX A

DETAILS OF PROCEDURE

Analysis of the Diode Matrix

Fig. IV-A, the three dimensional view of the diode matrix, can be reduced to Fig. V-A or V-B. By showing that points "A" and "B" on Fig. V-B are always at the same potential, the points may be connected for the purposes of static analysis. This reduction is valid, if the assumption of identical diodes is made, because the ratio of the number of back diodes to forward diodes in each of the two parallel leakage paths of Fig. V-B is the same.

It is obvious that as the matrix size is increased, more diodes are paralleled, lowering the ratio of the leakage path resistance to the read path resistance. Consequently, as N is increased, for a fixed readout current, the leakage paths take more and more of the total driver current. One important feature of memory design is design of the drivers, which, besides supplying readout current, must supply the leakage current. An important parameter for driver design is the ratio of leakage current (I_2) to readout current (I_1) as a function of matrix size. This curve was obtained using Sylvania-supplied low voltage characteristics for the diode 1N56A (Figs. X and XI) in conjunction with Fig. V-A.

The method used is as follows:

1. Assume a value of N.

2. Assume a value of leakage current.
3. In each of the three diode sections of the leakage path, divide the current in accordance with the number of parallel diodes. The voltage drop across the section is then the voltage across one diode in that section.
4. Using Fig. X and Fig. XI, add up the voltage drops in the leakage path. This voltage sum is the drop across the read diode.
5. I_1 is equal to (voltage drop across the read diode - .75) X (58.5) ma. This equation represents the slope and intercept of the forward characteristic curve of the diode. Published curves do not extend to the region of interest and they had to be extrapolated, but the diodes are usually stable up to 300 ma. D.C. and probably much higher for low duty cycles.
6. Calculate the desired ratios and the value of leakage current.

Leakage Current Voltage Analysis

As mentioned previously, all the cores in a z - plane are linked by the same output winding. When a word is read out, one core in that z - plane impresses on the output winding a voltage which is dependent upon the core state. Other cores in that z - plane, however, are pulsed by leakage currents, and they too impress a voltage

on the output winding. This leakage voltage appeared to be dependent upon the state of the core in the leakage circuit. The system under consideration allows the cores to be in any one of three states, "clear", "1", and "0" so that it became necessary to obtain in the laboratory the response of the core to small currents when the core was in all three states. Fig. IX-A shows a block diagram of the apparatus used.

A. The "0" State.

Driver #2 was disconnected. The output of driver #1 was raised sufficiently to put a test core in the "0" state, then was reduced to zero. The output was raised in small increments and for each increment, the core output voltage and the voltage across the metering resistor were recorded. Metering resistance voltage is proportional to the current pulsing the core, so that a spectrum of output voltage versus input current for a positively pulsed "0" was obtained. Ten windings were used on the input and twenty windings were used on the output. The input windings were then reversed and the same procedure followed to get the data for a negatively driven "clear".

B. The "1" State.

Driver #2 was disconnected after it was used to put the core in the "clear" state. Driver #1 output was raised to 100 ma.,

and then reduced to zero. The core was now in the "1" state. Driver #1 output was raised in small increments to 100 ma. and data was taken in the same manner as previously. The output was then raised to 110 ma. and the process repeated for the stable remanent state resulting from a 110 ma. positive pulse. Fig. IX-B is a plot of the data obtained in the laboratory.

Correlation of the Diode Matrix Analysis with Leakage Voltage Analysis

In analyzing the diode matrix, Fig. V-A was derived by connecting equipotential points "A" and "B" in Fig. V-B, with the ultimate goal of computing total leakage current as a function of N. In a leakage voltage analysis, the important criterian is the current in the individual diodes and their related cores, and it is not immediately obvious that the total leakage current in the matrix of Fig. V-A will produce the same effect. Consequently, the two leakage paths were kept separate, and Fig. V-B was used as a basis for this calculation.

In Fig. V-B, the number in brackets indicates the number of turns on the associated core through which the leakage current passes, and the sign indicates whether the output voltage tends to add or subtract from a read voltage. The resistances of the two leakage paths are in a ratio of N to (N-1). This is based on the assumption that for large matrices the currents in the two leakage branches and hence forward and back resistances in these branches are approximately equal.

One important result of the core data is that for small disturbances the voltage output of the core may be assumed to be independent of the state (see Fig. IX-B). This greatly simplified the computation of leakage current output voltage as a function of matrix size.

The leakage voltage in one parallel section of diodes is equal to the product of:

1. The current in one diode in that section.
2. The number of turns on the core through which this small leakage current passes.
3. The slope of the leakage current output voltage curve in volts per ampere-turn.
4. The number of diodes in that section.

However, the product of one and four yields the total leakage current in that section. The leakage voltage, then, is independent of the number of diodes in each section, and is dependent only on the leakage current. This establishes the conclusion that there is complete cancellation of leakage voltage in each parallel branch of Fig. V-B, which leaves a net leakage voltage of $I_2(N-1)(10)$.

In computing the leakage voltage as a function of N, the following procedure was followed:

1. I_2, the leakage current at 100 ma. read current, was recorded for each N curve shown on Fig. VII.

2. Leakage voltage equals $I_2(10)(.0963)$ where .0963 is the slope of the leakage current output voltage curve at small ampere-turn driving forces.

APPENDIX B

SUMMARY OF DATA AND CALCULATIONS

Figure VII shows the result of the diode matrix analysis. In addition to indicating at what read current the ratio of leakage current to read current is a minimum for a given value of N, it indicates the upward trend in the ratio as matrix size is increased. The silicon diode curve also clearly illustrates the advantages to be gained by its use.

To bring out trends more clearly, Figs. VIII and VIII-A were drawn from computed data. Fig. VIII shows what portion of the total driver current is taken by the leakage paths, and Fig. VIII-A shows how total leakage current increases with both matrix size and read current.

Fig.IX-B presents the laboratory data of the response of the core to small magnetizing forces. Two positions of the "1" state were used in order to investigate the possibility of improvement by choosing a better remanent point to store a "1".

Fig. VI shows the variation of leakage voltage with matrix size for a read current of 100 ma. Superimposed on this plot are the "1" and "0" output voltages for the system as it now operates.

APPENDIX C

SAMPLE CALCULATIONS

Analysis of the Diode Matrix

TABLE I

i_2	n	(n -1)	$\frac{i_2}{(n-1)}$	v_a	(2n -1)(n -1)
60ma	100	99	606	$.25^{V}$	19700

$\frac{i_2}{(2n-1)(n-1)}$	v_b (back)	(2n -1)	$\frac{i_2}{(2n-1)}$	v_c	v
3.1	2.5^{V}	199	300	$.195^{V}$	2.95^{V}

I_1	I_T	I_2/I_T	I_2/I_1
129ma	189ma	.318	.465

The values of v_a and v_c were obtained from Fig. X at points "A" and "C". The value of v_b was similarly obtained from Fig. XI at point B. The resultant point, $I_2/I_1 = .465$ at $I_1 = 129$ ma. for N = 100, is plotted on Fig. VII as point D. Values of I_2 were chosen so as to cover the region between 100ma. and the minimum of the resultant curve.

Calculation of Leakage Voltage

1. For N = 75 at I_1 = 100 ma., from Fig. VII, I_2 = 33 ma.
2. Leakage voltage = 33×10^{-3} (10)(.0963) = .0318 volts.

   This result is plotted on Fig. VI.

APPENDIX D

SUPPLEMENTAL DISCUSSION

Although all the previous work was predicated on an analysis of the static case, this by no means infers that the dynamic response of the system is of no importance. On the contrary, the dynamic case may impose even more stringent limitations on the expansion of the matrix, and before definite conclusions can be reached, this analysis should be carried out. Even without being mathematically rigorous, several general trends can be predicted.

Each leakage section in Fig. V-A can be replaced by an inductance in series with the parallel combination of a diode and a capacitance where:

1. The diode represents the resistance of all the parallel diodes in that section.
2. The capacitance represents the parallel combination of all diode shunt capacitance in that section.
3. The inductance represents the inductance of the cores through which the leakage current in that section passes.

The forward diode resistance and capacitance can be neglected, but the reverse diode resistance and capacitance is significant. Thus the entire leakage path can be represented by one inductance in series with the parallel combination of the net reverse diode resistance and the sum of the reverse diode capacitances. The read path can be

represented by the inductance of the core being read out, plus a series forward diode.

The core is driven by the current through its windings. For small matrices, C is small and may be considered an open circuit. Because of the high back resistance in the leakage circuit, the major portion of the driver current initially fires through the read path, reading out the core. As N is increased, there is a threefold effect:

1. Net back resistance decreases.
2. Net shunt capacity increases.
3. The net inductance in the leakage path decreases.

The read path circuit parameters are independent of N.

All three effects mentioned above are detrimental to the proper operation of the circuit, since they all tend to shunt more initial current through the leakage path, and thus reduce the current in the read path.

A mathematically rigorous analysis is impossible to do without laboratory data correlation because the shunt capacitance is variable with the back voltage across the diode. However, if the read path current rises too slowly, the core might not be read out. Generally speaking, if the rate of change of current in the read path is not equal to or greater than that in the leakage path, the system probably will not operate properly.

APPENDIX E

ORIGINAL DATA

See Figure IX-A for block diagram of apparatus .

Metering Resistors = 53 ohms
Input Turns = 10
Output Turns = 20

Pulse length = 2 microseconds
E_1 = Voltage across metering resistor
E = Voltage at output winding
I_1 = Input Current $= \frac{E_1}{53}$

"0" State			"1" State (110ma.)			Clear State		
E_1 (Volts)	I_1 (ma)	E_0 (Volts)	E_1 (Volts)	I_1 (ma)	E_0 (Volts)	E_1 (Volts)	I_1 (ma)	E_0 (Volts)
.225	4.24	.10	1.12	21.1	.45	.23	4.33	.09
.35	6.6	.15	2.25	42.4	1.05	.65	17.93	.25
.65	12.27	.25	3.52	66.4	1.95	.675	12.74	.27
.85	16.04	.30	4.66	87.8	2.90	.80	15.1	.29
1.4	26.4	.50	5.25	99.0	3.45	1.4	26.4	.50
1.5	28.3	.50	6.0	113.2	4.12	1.5	28.3	.55
2.0	37.7	.75	6.9	130.2	5.25	1.7	32.1	.64
2.5	47.2	.95				2.1	39.6	.75
2.95	55.7	1.02				2.35	44.3	.85
4.2	79.3	1.50				3.0	56.6	1.15
5.5	103.8	1.95				4.05	76.4	1.65
6.0	113.2	2.20	"1" State (100 ma.)			5.04	95.1	2.3
7.0	132.0	2.75	.54	10.2	.25	5.85	110.5	3.0
7.5	141.5	3.0	1.40	26.4	.56	6.6	124.5	3.75
8.0	151.0	3.3	2.40	45.3	1.00	7.5	141.5	4.75
8.5	160.5	3.5	3.46	65.3	1.60	8.25	155.8	6.3
10.4	196.3	4.5	4.30	81.2	2.16	8.75	165.0	11.0
13.5	255	5.0	5.10	96.2	2.70			
			5.60	105.8	3.20			

"1" State (120 ma.)		
.925	17.46	.40
1.70	32.10	.85
1.80	34.0	.90
3.08	58.1	1.70
4.45	83.9	2.85
6.35	119.8	4.75
6.37	120.1	4.80

APPENDIX F

BIBLIOGRAPHY

1. Bozorth, R.M., Ferromagnetism. D. Van Nostrand Company, Inc., New York, 1951, pages 539-543.

2. Final Development Report for Static Magnetic Storage with Non-destructive Readout. W.O. #800-36177. 15 December 1954, Contract NObsr 63348, General Electronics Laboratories, Inc., Cambridge, Mass.

3. Rajchman, J. A., A Myriabit Magnetic-Core Matrix Memory, Proceedings I.R.E., October 1953, Computer Issue, pages 1407-1421.

4. Freeman, J. R., Pulse Responses of Ferrite Memory Cores, Engineering Memorandum M-2568-1, Division 6, Lincoln Laboratory.

28791
K867 Krohn
A study of factors limiting the utility of a digital memory system with nondestructive read-out.

Thesis
28791
K867 Krohn
A study of factors limiting the utility of a digital memory system with nondestructive read-out.

thesK867
A study of factors limiting the utility
3 2768 002 11539 6
DUDLEY KNOX LIBRARY